Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.045”**

**PAD FUNCTIONS:**

1. **A0**
2. **B0**
3. **O0**
4. **A1**
5. **B1**
6. **O1**
7. **GND**
8. **O3**
9. **B3**
10. **A3**
11. **O2**
12. **B2**
13. **A2**
14. **VCC**

**8 7**

**9**

**10**

**11**

**12**

**13 14 1**

**6**

**5**

**4**

**3**

**2**

**74F08**

**MASK**

**REF**

**.048”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: GND or FLOAT**

**Mask Ref: 74F08**

**APPROVED BY: DK DIE SIZE .045” X .048” DATE: 6/28/22**

**MFG: MOTOROLA THICKNESS .015” P/N: 54F08**

**DG 10.1.2**

#### Rev B, 7/19/02